ElanSC400 Verification Board Schematics

Table of Contents

Rev 1.0: Original design

Rev 1.1:
Sh. 11: Corrected CAD for ISA Bus connector.

Rev 2.0:
Sh.2: Added 0.01uF & 0.001uF caps to ElanSC400 power planes.
Added pads to bottom of board for caps near SC400 socket.
Sh.3: Removed VCC5 from analyzer headers.
Removed RESET# from analyzer header P19.
Added GND to NI-1 & NI-2 connectors.
Added RESET# to NI-2 connector.
Sh.4: Changed SW5 & SW6 from an Omron B3S1000 to a C&K KT11P2SM.
Changed LFx circuit from a one component to three component design.
Added GND to P27 for RESET#.
Sh.6: Added VL device VDD & VEE controls to P20.
Added VCC5 to P23.
Sh.7: Changed RS1-RS7 to sets of 0 ohm resistors.
Sh.8: Changed pull-ups on BIOSCS#, DIAGCS#, & X16CS# from VCCROM5 to VCC3.
Sh.9: Added ROMID2 to P42.
Sh.10: Added KBDROW10 (BALE) to buffer U24.
Sh.11: Added buffered ISABALE to ISA connector P34 & P35.
Changed SA20-25 on U9 to buffered BSA20-25.
Changed pull-ups on IOCHRDY, KBDROW12 (MCS16#), & IOCS16# from VCCISA5 to VCC3.
Sh.12: Changed VCC for U22 from VCCISA5 to VCC3.
Changed pull-ups on PCMCIA card detects for slot A & slot B from VCCISA5 to VCC3.
Sh.13: Added work-around for SC400 IrDA errata to invert TXD & RXD.
Sh.14: Changed pull-ups on PPOEN# & PPWE# from VCCISA5 to VCC3.
Added pull-ups to VCC3 on STRB#, AFDT#, INIT#, & SLCTIN#.
Sh.15: Added ROMID2 to U10.
Sh.18: Changed P12 from an AMP right angle 749265-1 to an AMP vertical 750329-2.
Added circuit to translate 5 volt input to the SC400 to 3.3 volts.
Sh.19: Changed circuit for PSLVEE to support VL-bus devices also.
Sh.20: Changed position & pinout of P6 & P7 for power supply module.
Added circuit for support of an external back-up battery.
Added bulk caps for P5VOLT, P12VOLT, VCCCPU, VCCANLG3, VEEPOS, & VEENEG.

Title	ElanSC400 Verification Board	
Size	Document Number H2.SCH	Rev 2.0
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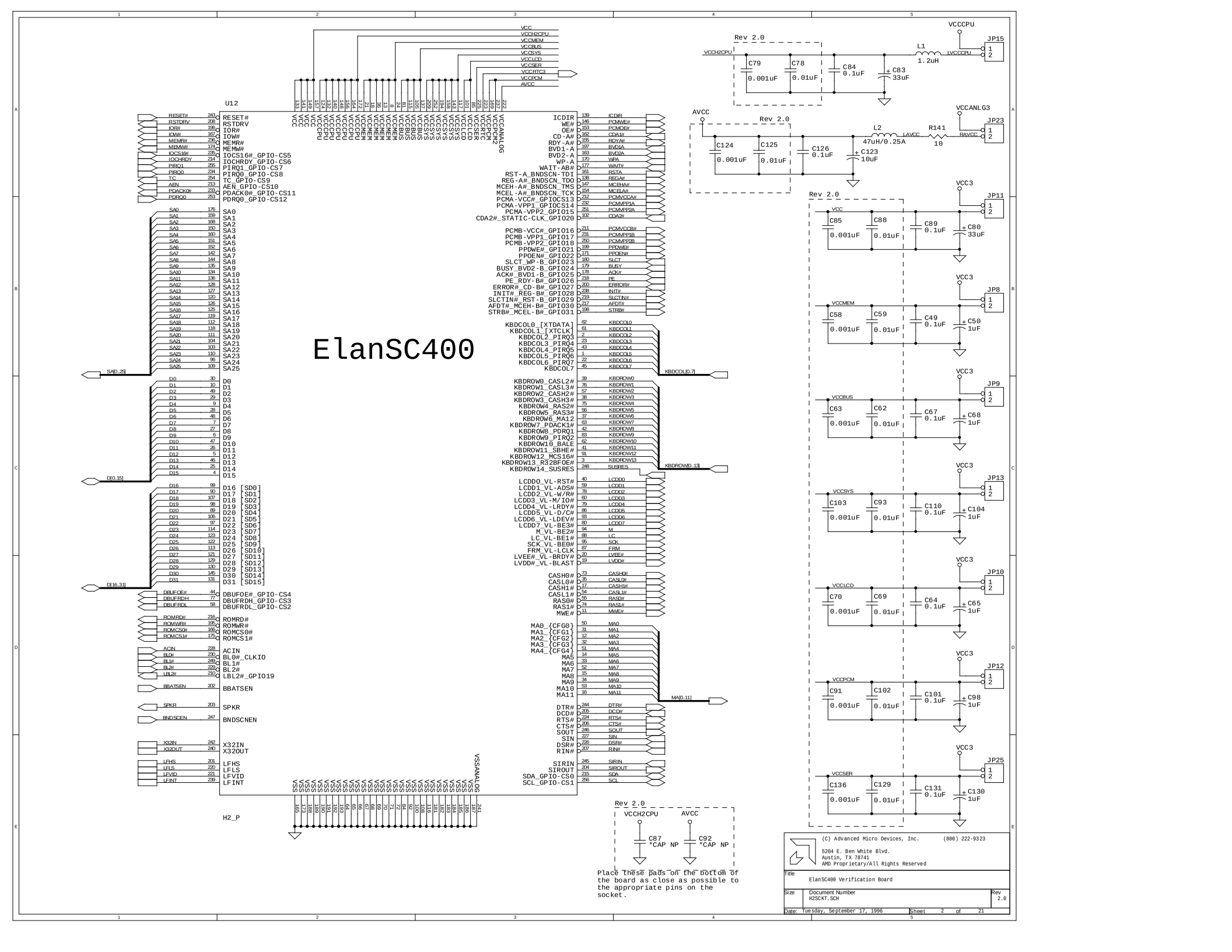
ElanSC400
U12
VCC
VCCH2CPU
VCCMEM
VCCBUS
VCCSYS
VCCLCD
VCCSER
VCCRTC3
VCCPCM
AVCC
VCCPCM2
VCCANALOG
VSSANALOG
RESET#
RSTDRV
IOR#
IOW#
MEMR#
MEMW#
IOCS16#_GPIO-CS5
IOCHRDY_GPIO-CS6
PIRQ1_GPIO-CS7
PIRQ0_GPIO-CS8
TC_GPIO-CS9
AEN_GPIO-CS10
PDACK0#_GPIO-CS11
PDRQ0_GPIO-CS12
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
SA8
SA9
SA10
SA11
SA12
SA13
SA14
SA15
SA16
SA17
SA18
SA19
SA20
SA21
SA22
SA23
SA24
SA25
SA[0..25]
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D[0..15]
D16 [SD0]
D17 [SD1]
D18 [SD2]
D19 [SD3]
D20 [SD4]
D21 [SD5]
D22 [SD6]
D23 [SD7]
D24 [SD8]
D25 [SD9]
D26 [SD10]
D27 [SD11]
D28 [SD12]
D29 [SD13]
D30 [SD14]
D31 [SD15]
D[16..31]
DBUFOE#_GPIO-CS4
DBUFRDH_GPIO-CS3
DBUFRDL_GPIO-CS2
ROMRD#
ROMWR#
ROMCS0#
ROMCS1#
ACIN
BL0#_CLKIO
BL1#
BL2#
LBL2#_GPIO19
BBATSEN
SPKR
BNDSCNEN
X32IN
X32OUT
LFHS
LFLS
LFVID
LFINT
H2_P
ICDIR
WE#
OE#
CD-A#
RDY-A#
BVD1-A
BVD2-A
WP-A
WAIT-AB#
RST-A_BNDSCN-TDI
REG-A#_BNDSCN_TDO
MCEH-A#_BNDSCN_TMS
MCEL-A#_BNDSCN_TCK
PCMA-VCC#_GPIOCS13
PCMA-VPP1_GPIOCS14
PCMA-VPP2_GPIO15
CDA2#_STATIC-CLK_GPIO20
PCMB-VCC#_GPIO16
PCMB-VPP1_GPIO17
PCMB-VPP2_GPIO18
PPDWE#_GPIO21
PPOEN#_GPIO22
SLCT_WP-B_GPIO23
BUSY_BVD2-B_GPIO24
ACK#_BVD1-B_GPIO25
PE_RDY-B#_GPIO26
ERROR#_CD-B#_GPIO27
INIT#_REG-B#_GPIO28
SLCTIN#_RST-B_GPIO29
AFDT#_MCEH-B#_GPIO30
STRB#_MCEL-B#_GPIO31
KBDCOL0_[XTDATA]
KBDCOL1_[XTCLK]
KBDCOL2_PIRQ3
KBDCOL3_PIRQ4
KBDCOL4_PIRQ5
KBDCOL5_PIRQ6
KBDCOL6_PIRQ7
KBDCOL7
KBDCOL[0..7]
KBDROW0_CASL2#
KBDROW1_CASL3#
KBDROW2_CASH2#
KBDROW3_CASH3#
KBDROW4_RAS2#
KBDROW5_RAS3#
KBDROW6_MA12
KBDROW7_PDACK1#
KBDROW8_PDRQ1
KBDROW9_PIRQ2
KBDROW10_BALE
KBDROW11_SBHE#
KBDROW12_MCS16#
KBDROW13_R32BFOE#
KBDROW14_SUSRES
KBDROW[0..13]
LCDD0_VL-RST#
LCDD1_VL-ADS#
LCDD2_VL-W/R#
LCDD3_VL-M/IO#
LCDD4_VL-LRDY#
LCDD5_VL-D/C#
LCDD6_VL-LDEV#
LCDD7_VL-BE3#
M_VL-BE2#
LC_VL-BE1#
SCK_VL-BE0#
FRM_VL-LCLK
LVEE#_VL-BRDY#
LVDD#_VL-BLAST
CASH0#
CASL0#
CASH1#
CASL1#
RAS0#
RAS1#
MWE#
MA0_{CFG0}
MA1_{CFG1}
MA2_{CFG2}
MA3_{CFG3}
MA4_{CFG4}
MA5
MA6
MA7
MA8
MA9
MA10
MA11
MA[0..11]
DTR#
DCD#
RTS#
CTS#
SOUT
SIN
DSR#
RIN#
SIRIN
SIROUT
SDA_GPIO-CS0
SCL_GPIO-CS1
Rev 2.0
VCCH2CPU
AVCC
C87
*CAP NP
C92
*CAP NP
Place these pads on the bottom of the board as close as possible to the appropriate pins on the socket.
VCCCPU
JP15
L1
1.2uH
LVCCCPU
C79
0.001uF
C78
0.01uF
C84
0.1uF
C83
33uF
VCCANLG3
JP23
L2
47uH/0.25A
LAVCC
R141
10
RAVCC
C124
0.001uF
C125
0.01uF
C126
0.1uF
C123
10uF
VCC3
JP11
C85
0.001uF
C88
0.01uF
C89
0.1uF
C80
33uF
JP8
C58
0.001uF
C59
0.01uF
C49
0.1uF
C50
1uF
JP9
C63
0.001uF
C62
0.01uF
C67
0.1uF
C68
1uF
JP13
C103
0.001uF
C93
0.01uF
C110
0.1uF
C104
1uF
JP10
C70
0.001uF
C69
0.01uF
C64
0.1uF
C65
1uF
JP12
C91
0.001uF
C102
0.01uF
C101
0.1uF
C98
1uF
JP25
C136
0.001uF
C129
0.01uF
C131
0.1uF
C130
1uF
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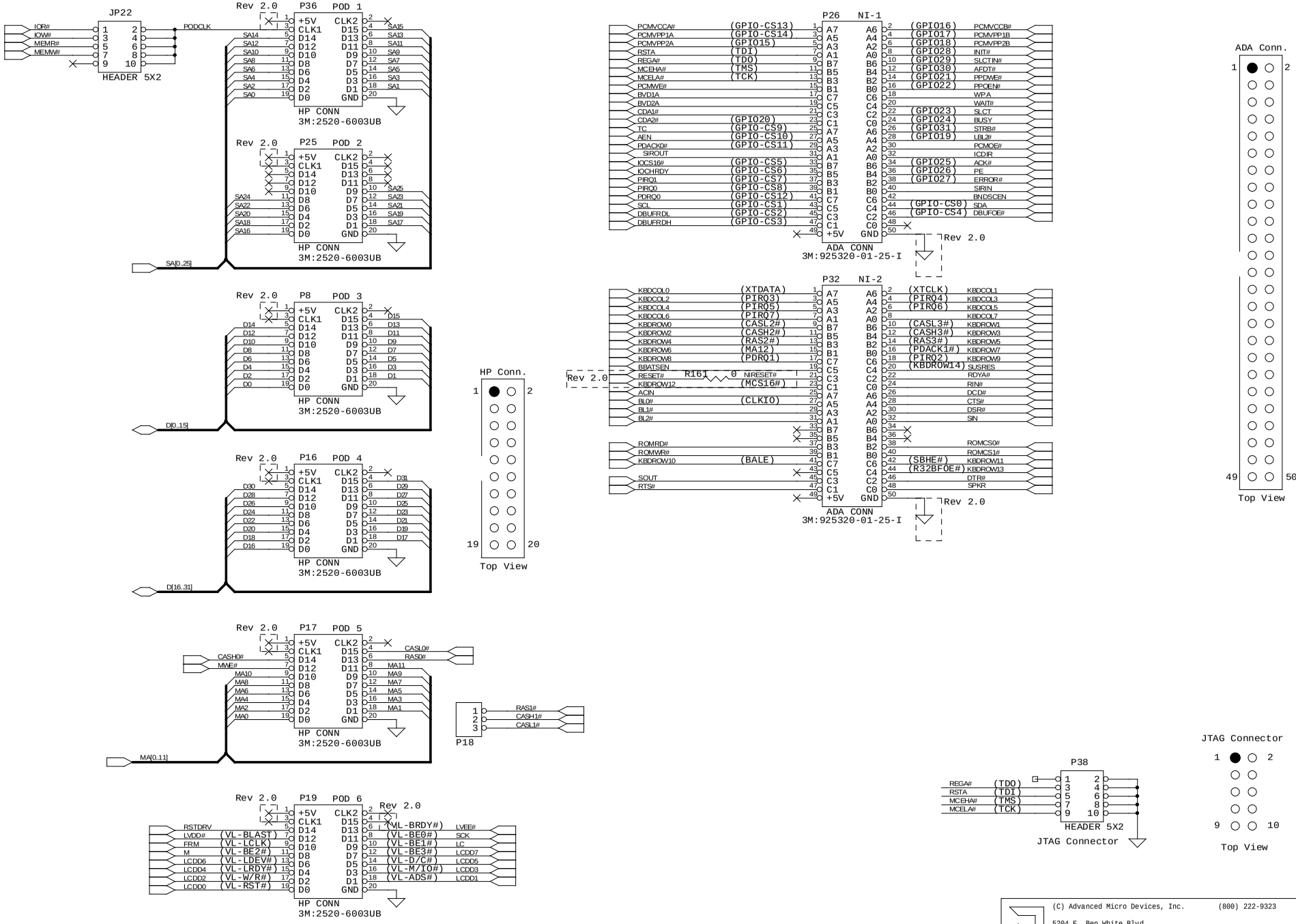

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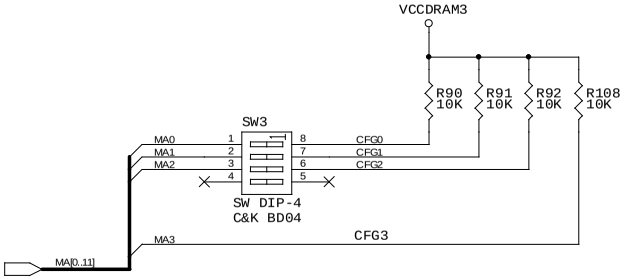


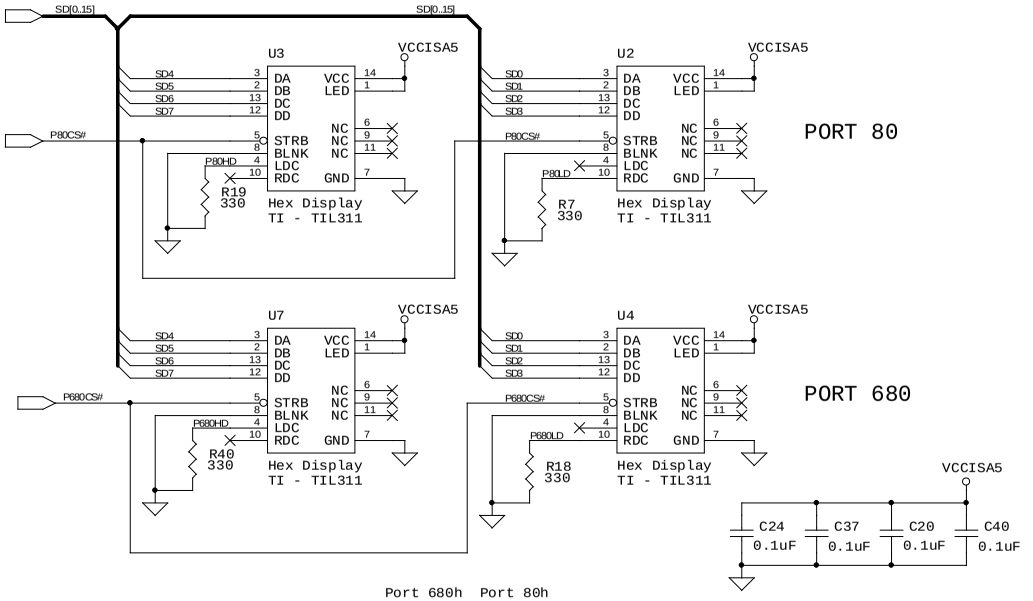
H2 PIN STRAP OPTIONS

CFG1 CFG0 Configuration
0 0 x8 ROMCS0# ROM Interface
1 0 x16 ROMCS0# ROM Interface
1 1 x32 ROMCS0# ROM Interface

CFG2 Configuration
0 Enable ROMCS0# decode on the ROMCS0# pin.
1 Enable ROMCS0# decode to access PCMCIA socket A.

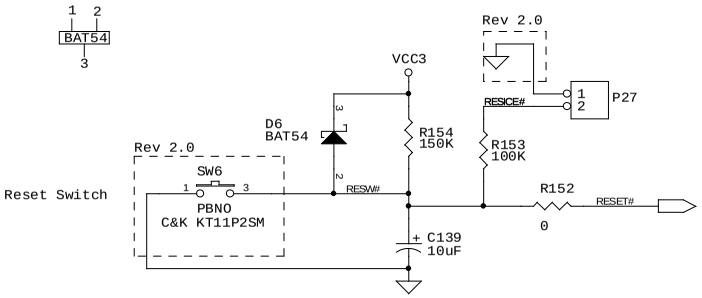
CFG3 Configuration
0 Enable GPIO-CS(4:2) signals.
1 Enable SD buffer controls.

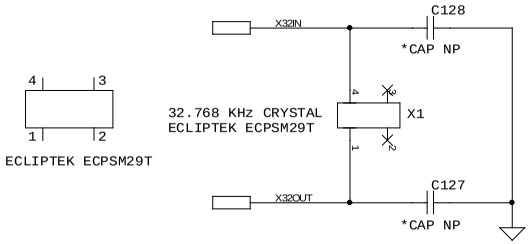
CFG4 Configuration
0 Disable Boundary Scan Function.
1 Enable Boundary Scan Function.

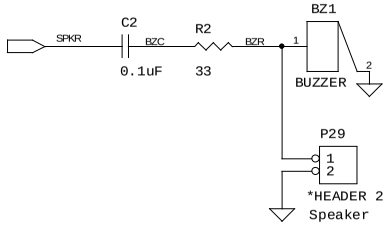


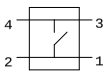
NOTE:
Place the 680h displays before the 80h displays if possible. See diagram.

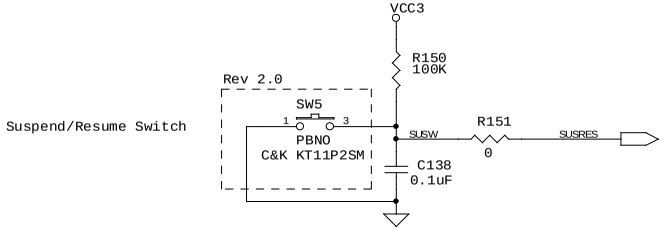
Port 680h: U7 U4
Port 80h: U3 U2

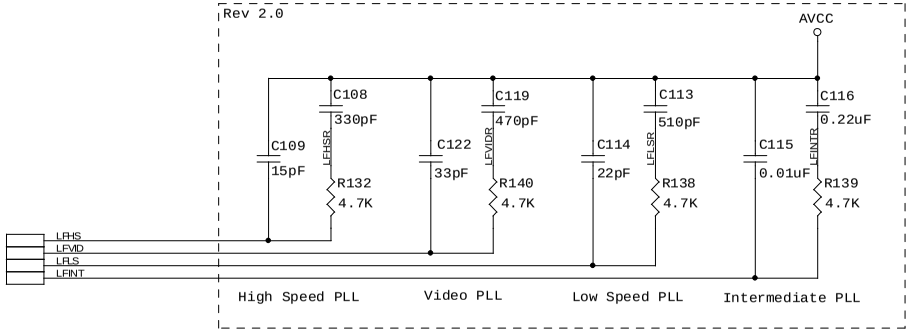


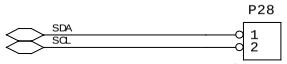












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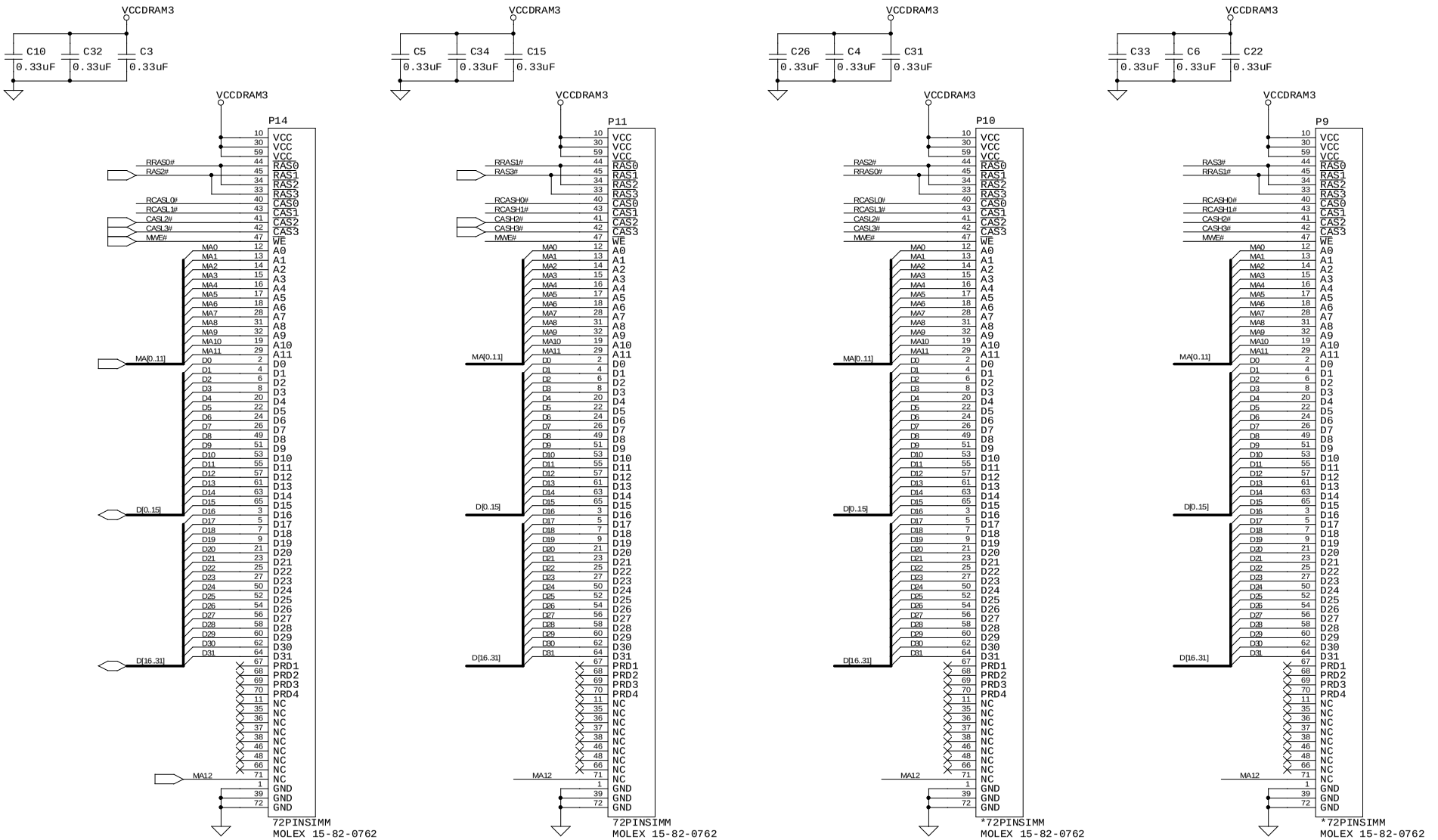

RAS0# R43 0 RRAS0#
RAS1# R44 0 RRAS1#

CASL0# R42 0 RCASL0#
CASL1# R45 0 RCASL1#

CASH0# R41 0 RCASH0#
CASH1# R46 0 RCASH1#

3.3 Volt SIMMS Only

NOTE:
Using 4Mx4 DRAM in a 64MB system will exceed the loading requirements of the MWE# and MA signals. ElanSC400 will need to be programmed to support this configuration.

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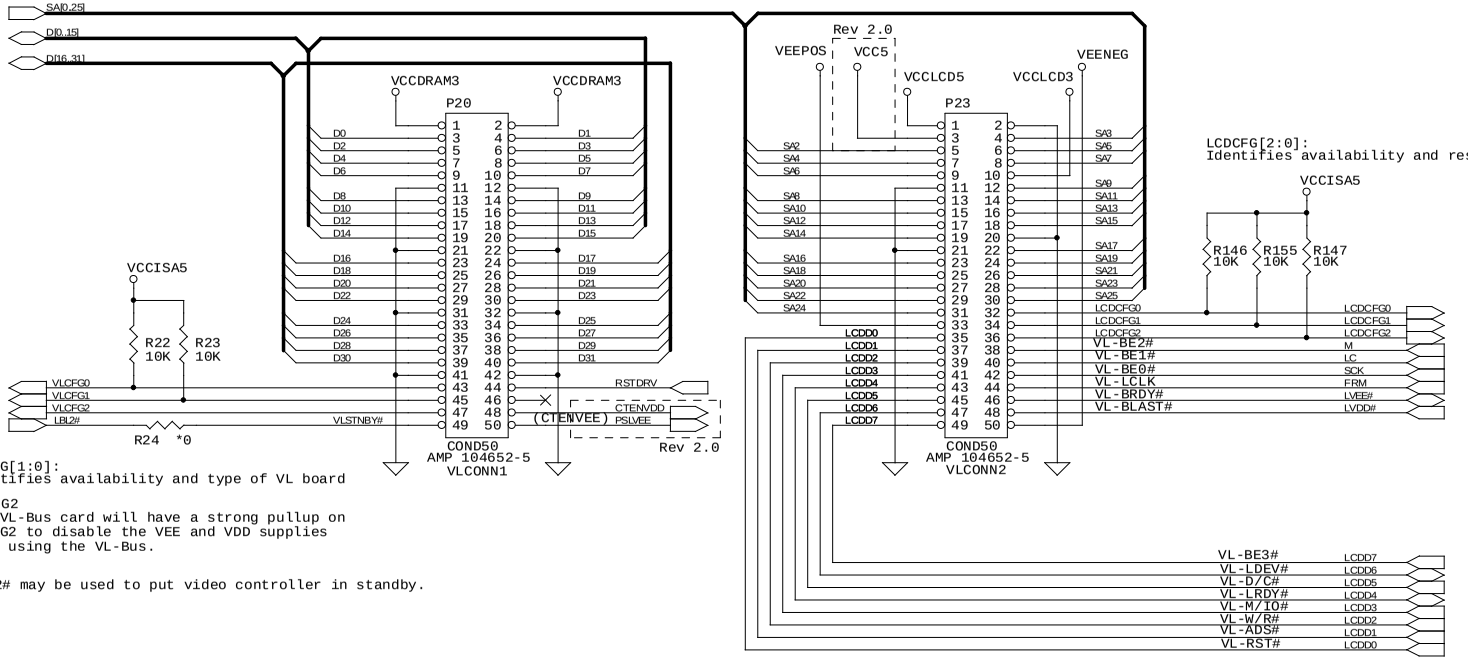
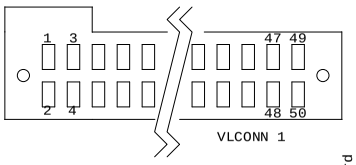


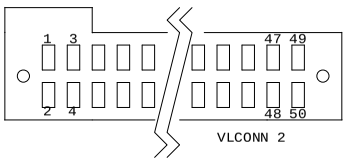
VLCFG[1:0]:
Identifies availability and type of VL board

VLCFG2
The VL-Bus card will have a strong pullup on VLCFG2 to disable the VEE and VDD supplies when using the VL-Bus.

LBL2# may be used to put video controller in standby.



Edge of Board



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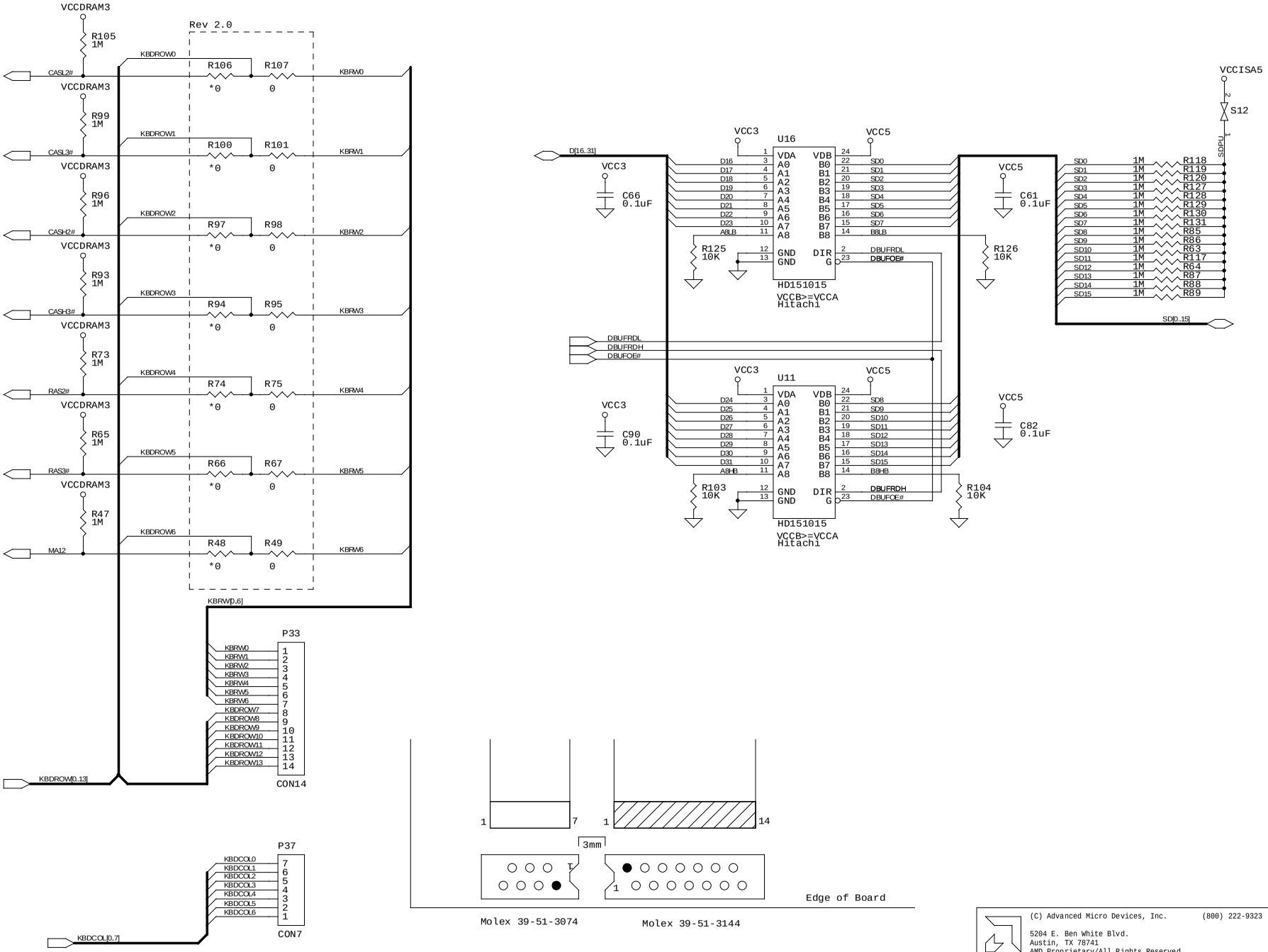

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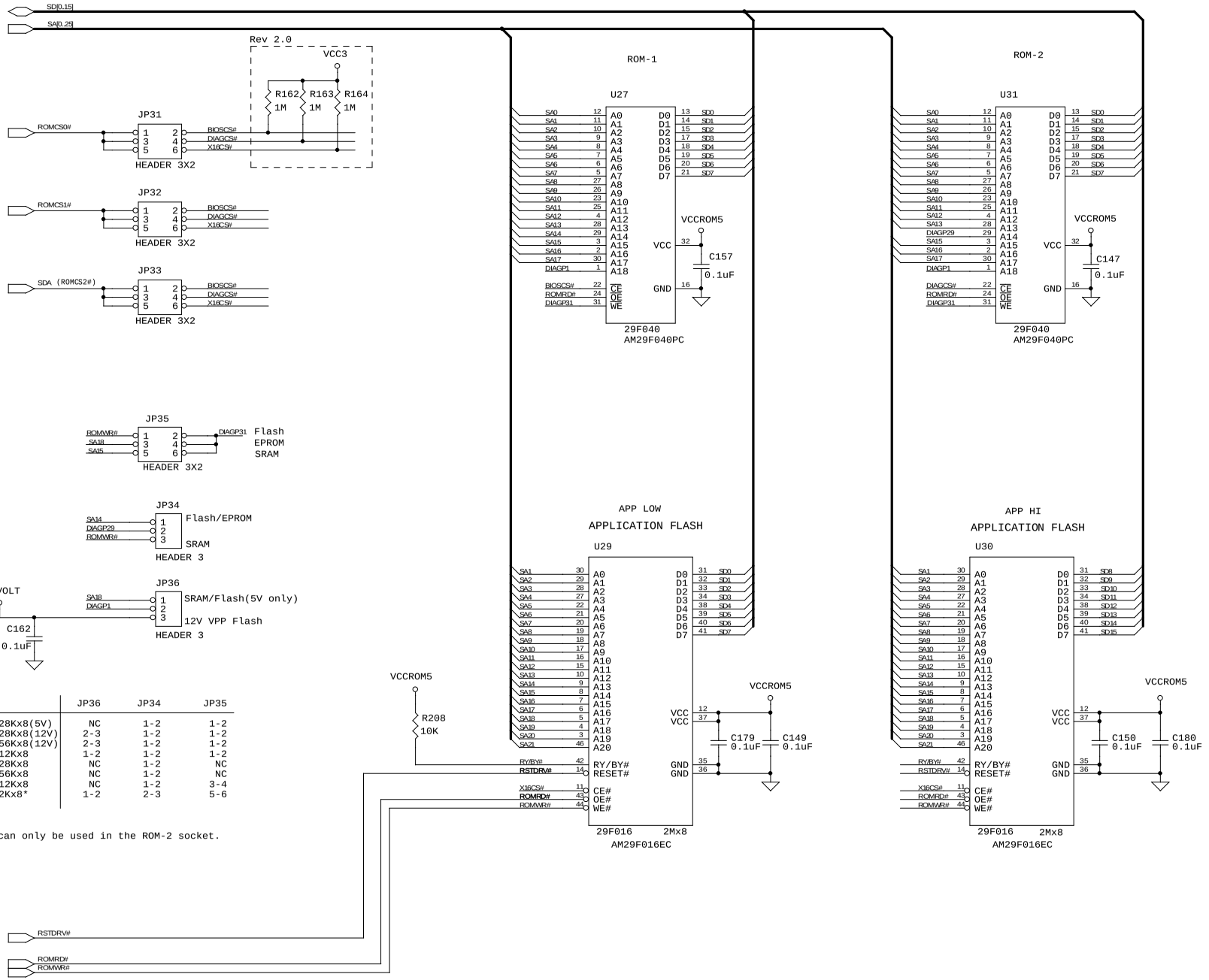

Device	JP36	JP34	JP35
Flash 128Kx8(5V)	NC	1-2	1-2
Flash 128Kx8(12V)	2-3	1-2	1-2
Flash 256Kx8(12V)	2-3	1-2	1-2
Flash 512Kx8	1-2	1-2	1-2
EPROM 128Kx8	NC	1-2	NC
EPROM 256Kx8	NC	1-2	NC
EPROM 512Kx8	NC	1-2	3-4
SRAM 512Kx8*	1-2	2-3	5-6

* SRAM can only be used in the ROM-2 socket.

Title: ElanSC400 Verification Board

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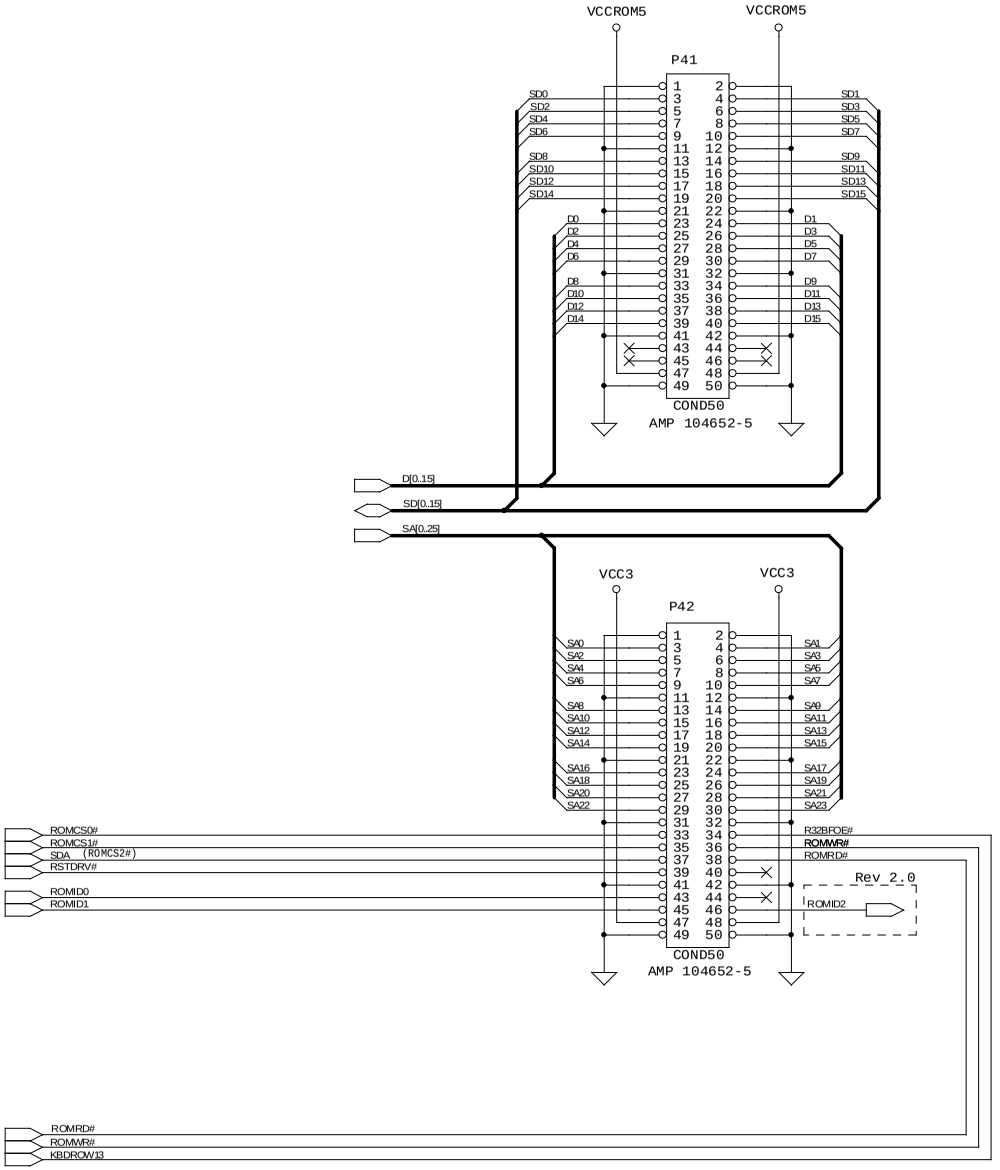

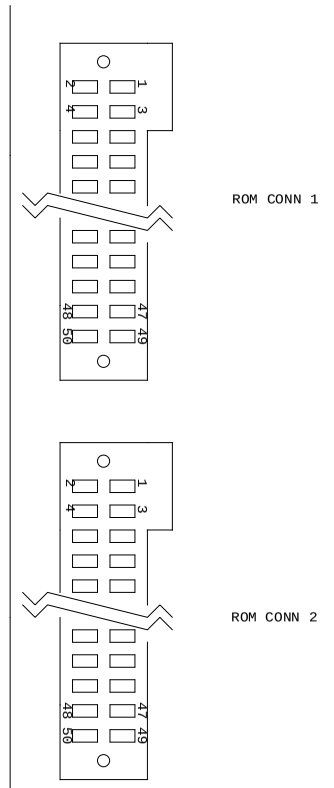

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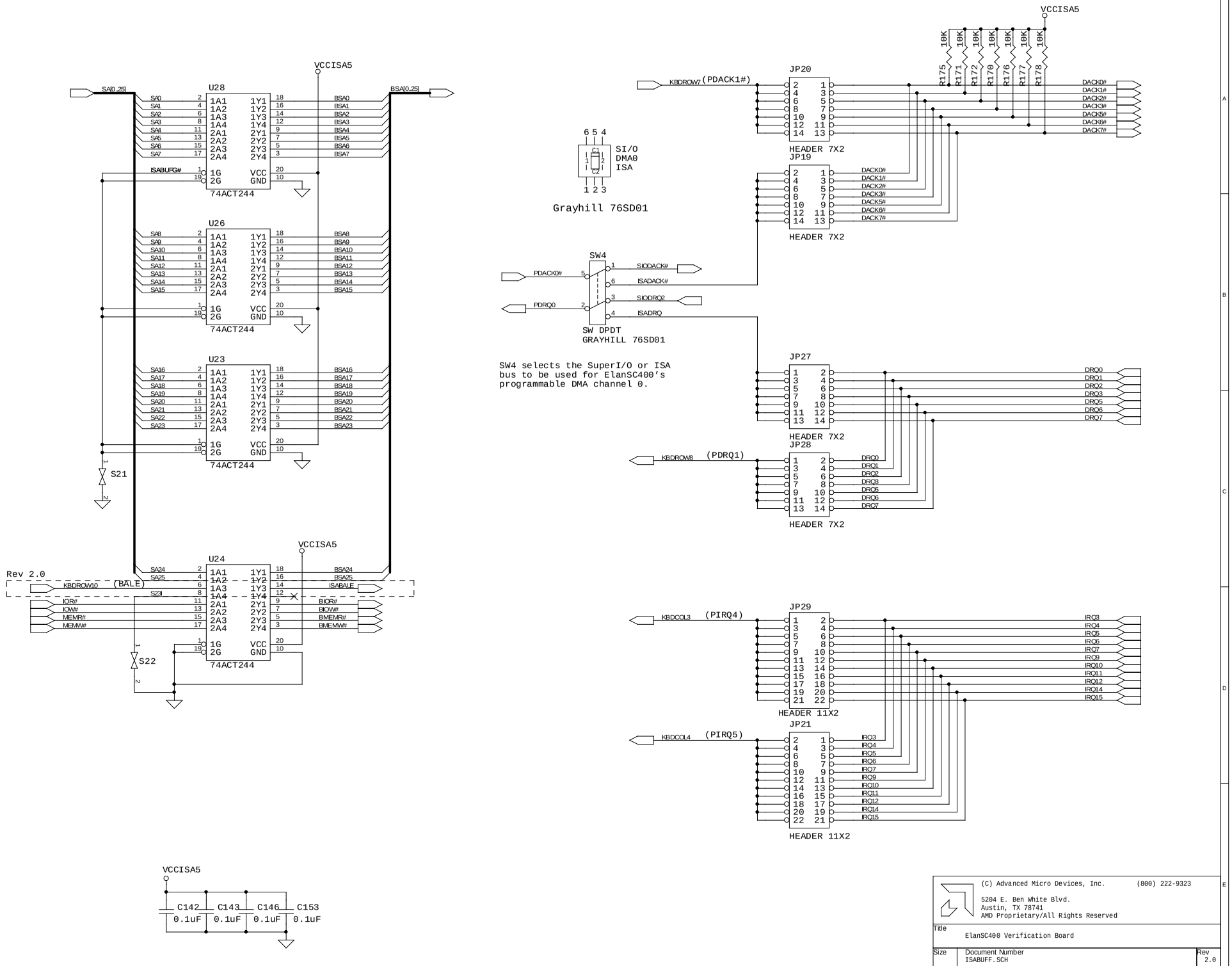

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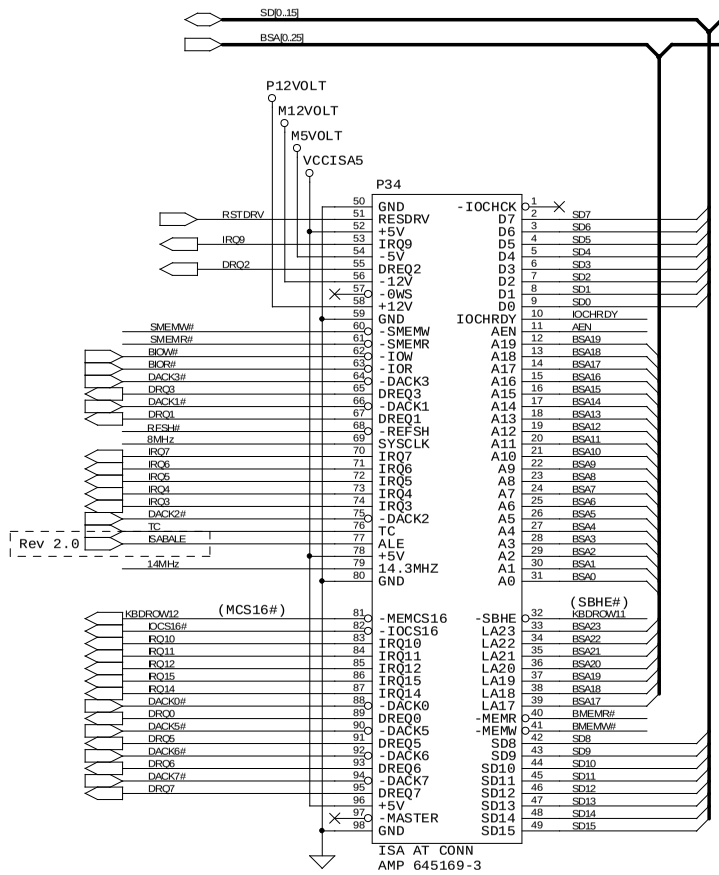
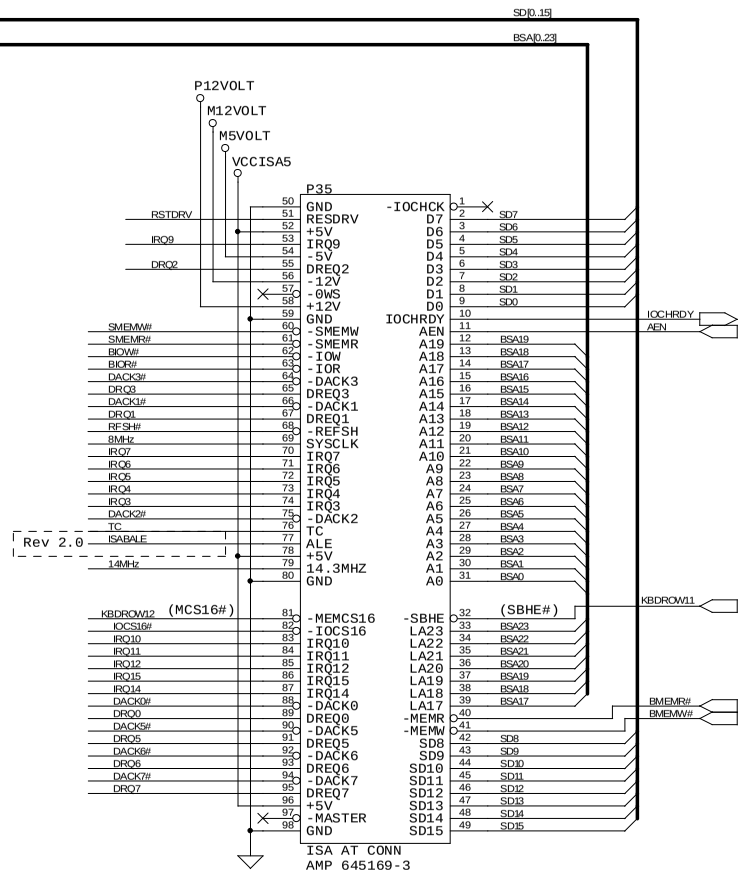
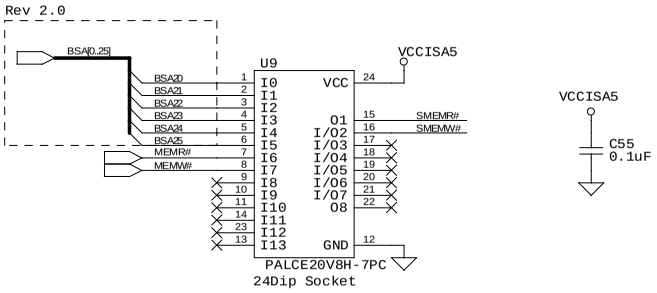
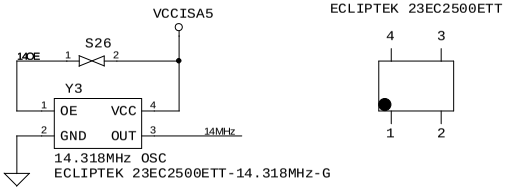
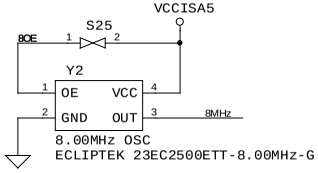


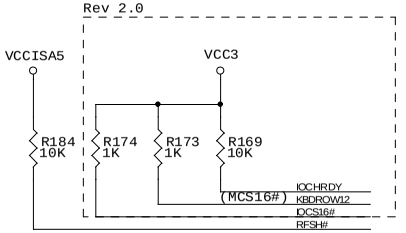




PAL equations
SMEMR# = /BSA20 * /BSA21 * /BSA22 * /BSA23 * /BSA24 * /BSA25 * /MEMR#
SMEMW# = /BSA20 * /BSA21 * /BSA22 * /BSA23 * /BSA24 * /BSA25 * /MEMW#







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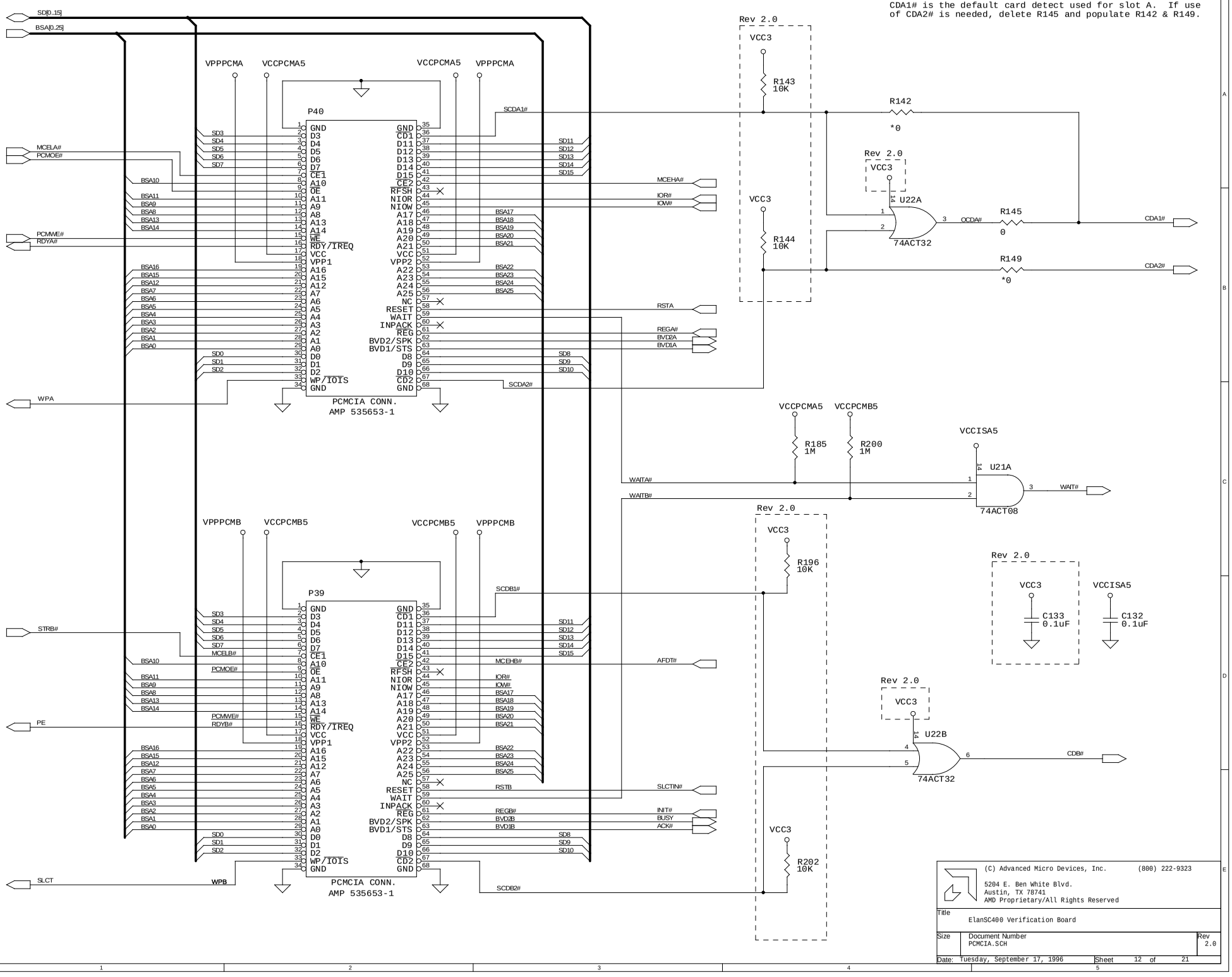
CDA1# is the default card detect used for slot A. If use of CDA2# is needed, delete R145 and populate R142 & R149.
SD[0..15]
BSA[0..25]
VPPPCMA
VCCPCMA5
VCCPCMA5
VPPPCMA
P40
PCMCIA CONN.
AMP 535653-1
MCELA#
PCMOE#
PCMWE#
RDYA#
WPA
SCDA1#
SCDA2#
MCEHA#
IOR#
IOW#
RSTA
REGA#
BVD2A
BVD1A
Rev 2.0
VCC3
R143
10K
R142
*0
R144
10K
R145
0
R149
*0
U22A
74ACT32
OCDA#
CDA1#
CDA2#
VCCPCMA5
VCCPCMB5
VCCISA5
R185
1M
R200
1M
U21A
74ACT08
WAITA#
WAITB#
WAIT#
VPPPCMB
VCCPCMB5
VCCPCMB5
VPPPCMB
P39
PCMCIA CONN.
AMP 535653-1
STRB#
PE
SLCT
WPB
SCDB1#
SCDB2#
MCEHB#
AFDT#
IOR#
IOW#
RSTB
SLCTIN#
REGB#
BVD2B
BVD1B
INIT#
BUSY
ACK#
R196
10K
R202
10K
C133
0.1uF
C132
0.1uF
U22B
74ACT32
CDB#
(C) Advanced Micro Devices, Inc. (800) 222-9323
5204 E. Ben White Blvd.
Austin, TX 78741
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Title
ElanSC400 Verification Board
Size
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Rev
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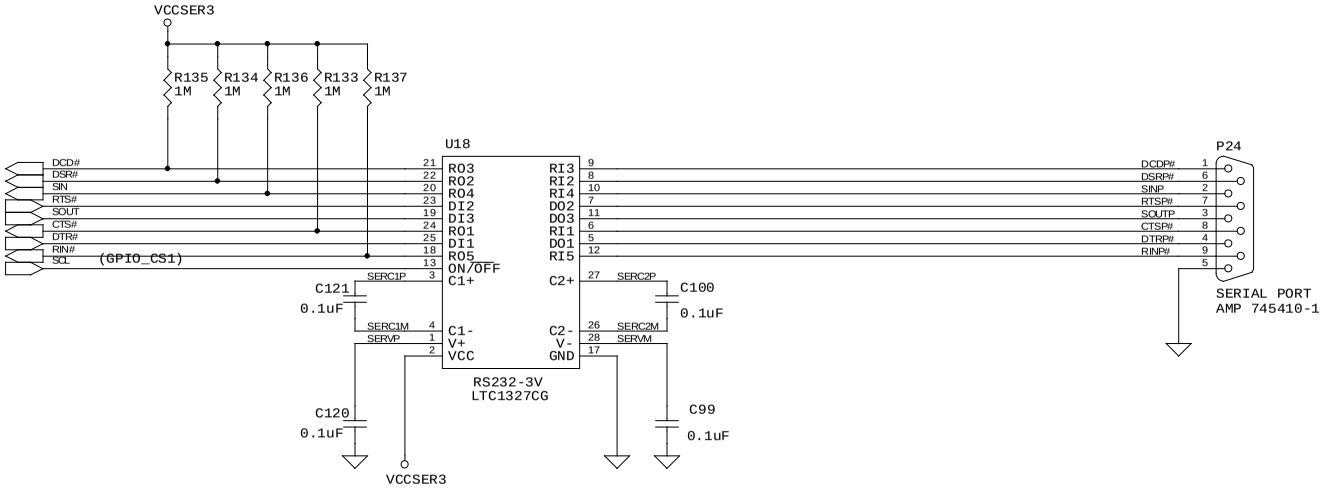
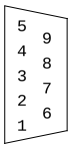
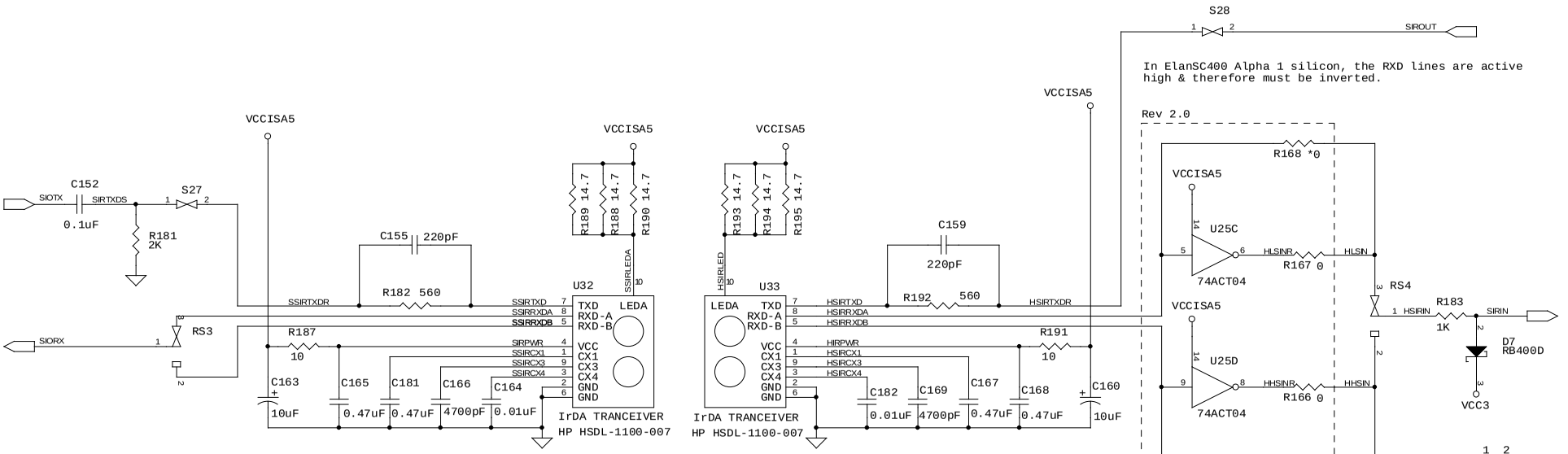
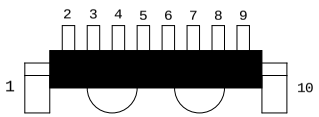
Elan SC400 Serial Port



Serial Connector







HSDL-1100-007

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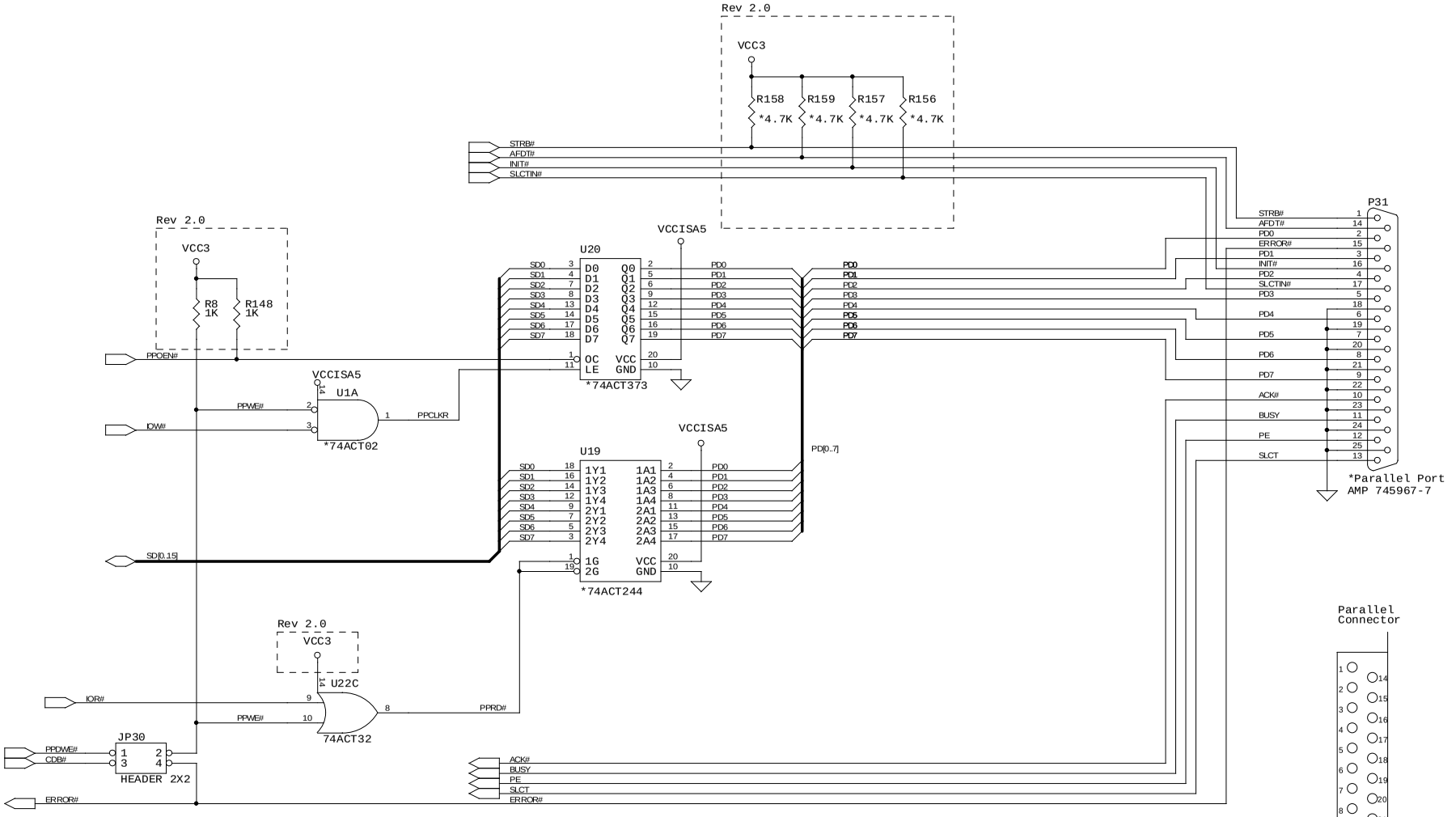
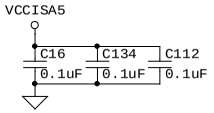


The group of ElanSC400 pins GPIO16-31 are available for the following functions: GPIO16-31, PCMCIA Slot B, or Parallel Port. Refer to the table below for JP32 settings for the listed functions.

Function	JP30
GPIO	NC
PCMCIA Slot B	3-4
Parallel Port	1-2

When PCMCIA Socket B is selected, PPOEN# and PPDWE# are tri-stated.

R8 and R148 are needed, to eliminate the possibility of data contention from the parallel port.



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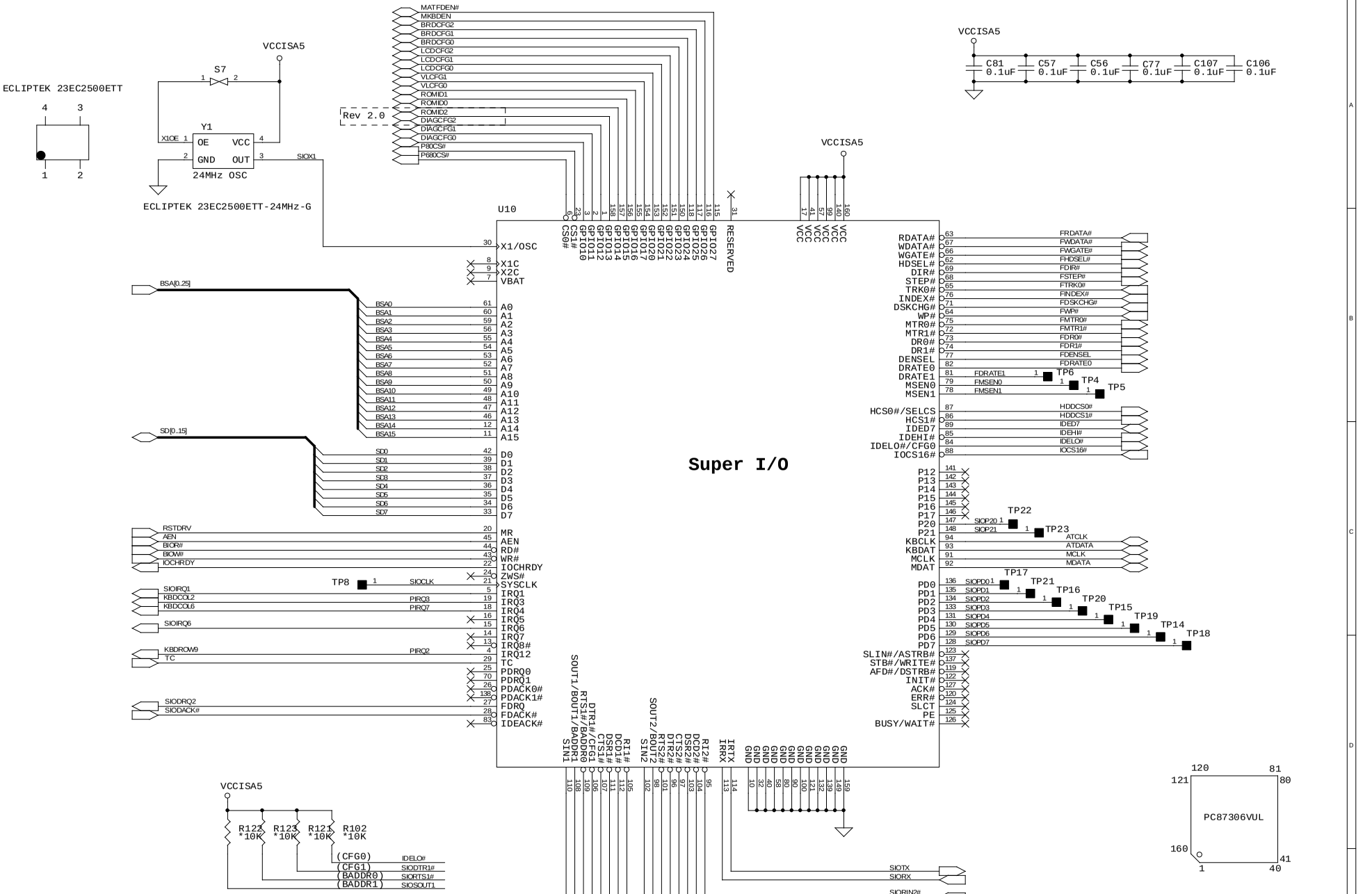

87306 CONFIGURATION STRAPS

CFG1	CFG0	RESET CONFIGURATION
0	0	Primary FDC & IDE,LPT1,COM1,GPIO Port 1 & Port 2 @78/9h,KBC with X1/3 clock,RTC
0	1	Reserved
1	0	Primary FDC,LPT1,COM1,(Non-IR) COM2,KBC with X1/3 clock,RTC
1	1	All modules disabled

BADDR1	BADDR0	INDEX	DATA
0	0	398	399
0	1	26E	26F
1	0	15C	15D
1	1	02E	02F

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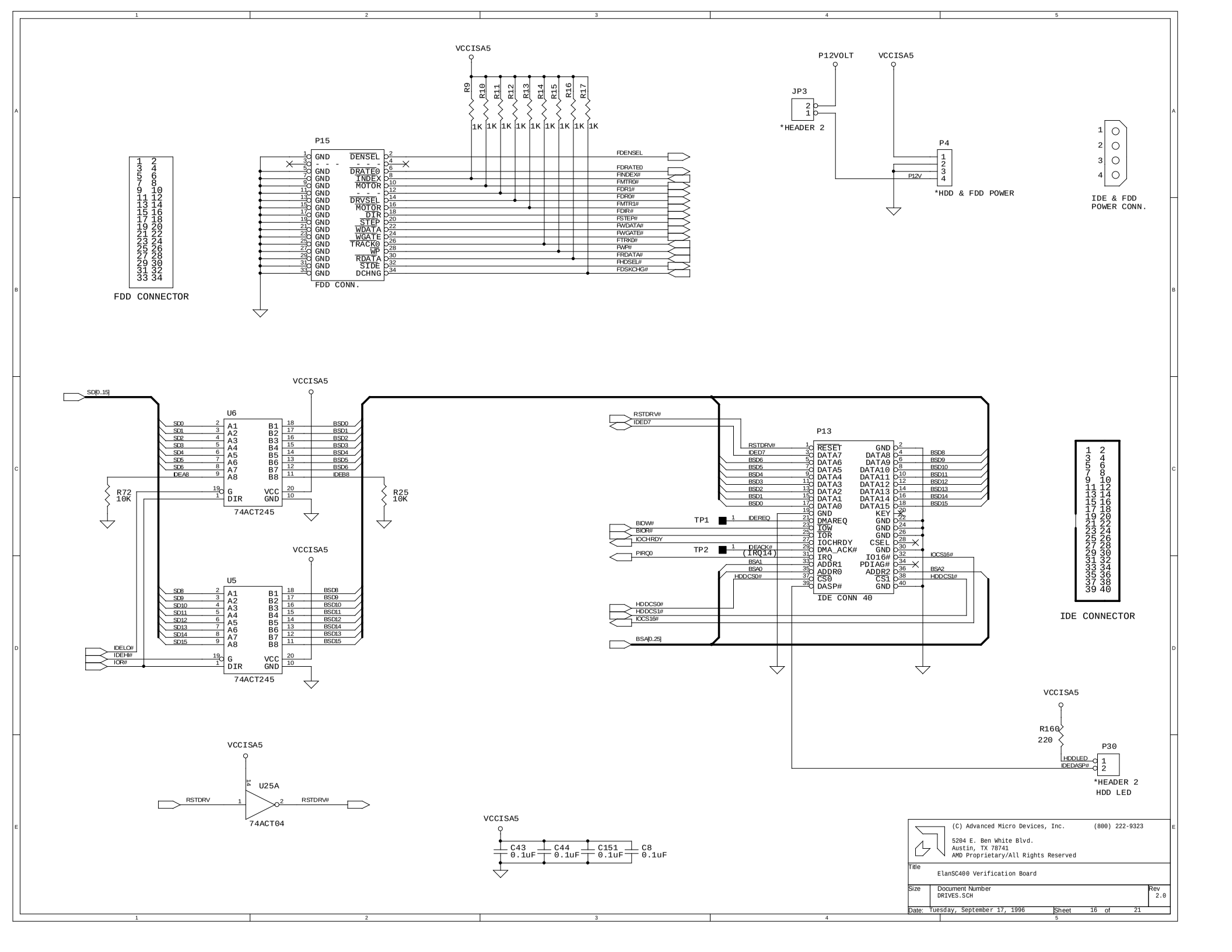
FDD CONNECTOR
P15
FDD CONN.
VCCISA5
R9 R10 R11 R12 R13 R14 R15 R16 R17
1K
GND DENSEL
DRATE0
INDEX
MOTOR
DRVSEL
MOTOR
DIR
STEP
WDATA
WGATE
TRACK0
WP
RDATA
SIDE
DCHNG
FDENSEL
FDRATE0
FINDEX#
FMTR0#
FDR1#
FDR0#
FMTR1#
FDIR#
FSTEP#
FWDATA#
FWGATE#
FTRK0#
FWP#
FRDATA#
FHDSEL#
FDSKCHG#
P12VOLT
VCCISA5
JP3
*HEADER 2
P4
P12V
*HDD & FDD POWER
IDE & FDD
POWER CONN.
SD[0..15]
U6
74ACT245
R72
10K
R25
10K
U5
IDELO#
IDEHI#
IOR#
RSTDRV#
IDED7
P13
IDE CONN 40
TP1
IDEREQ
TP2
DEACK#
(IRQ14)
BIOW#
BIOR#
IOCHRDY
PIRQ0
HDDCS0#
HDDCS1#
IOCS16#
BSA[0..2]
IDE CONNECTOR
R160
220
P30
HDDLED
IDEDASP#
*HEADER 2
HDD LED
U25A
74ACT04
RSTDRV
RSTDRV#
C43 C44 C151 C8
0.1uF
(C) Advanced Micro Devices, Inc. (800) 222-9323
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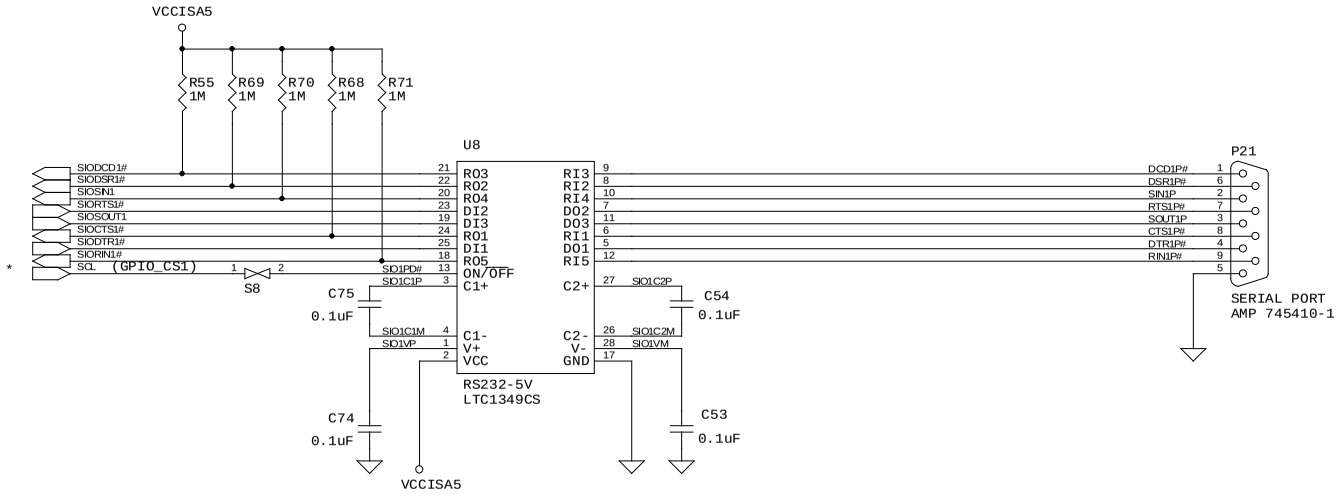
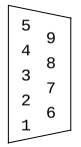
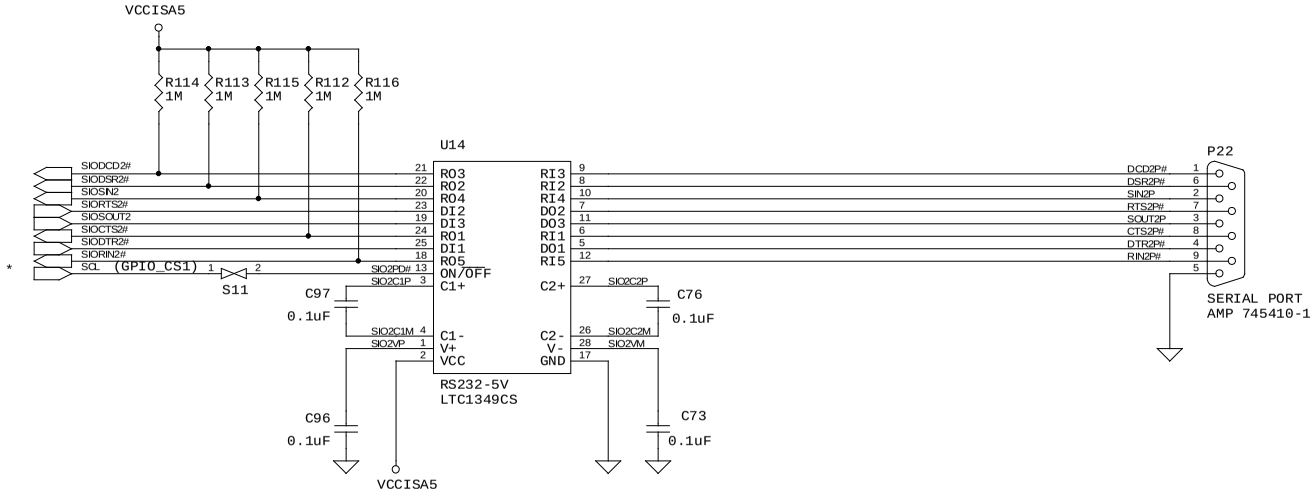


Serial Connector





* When turning off VCCISA5, make sure SCL is low to prevent current draw.

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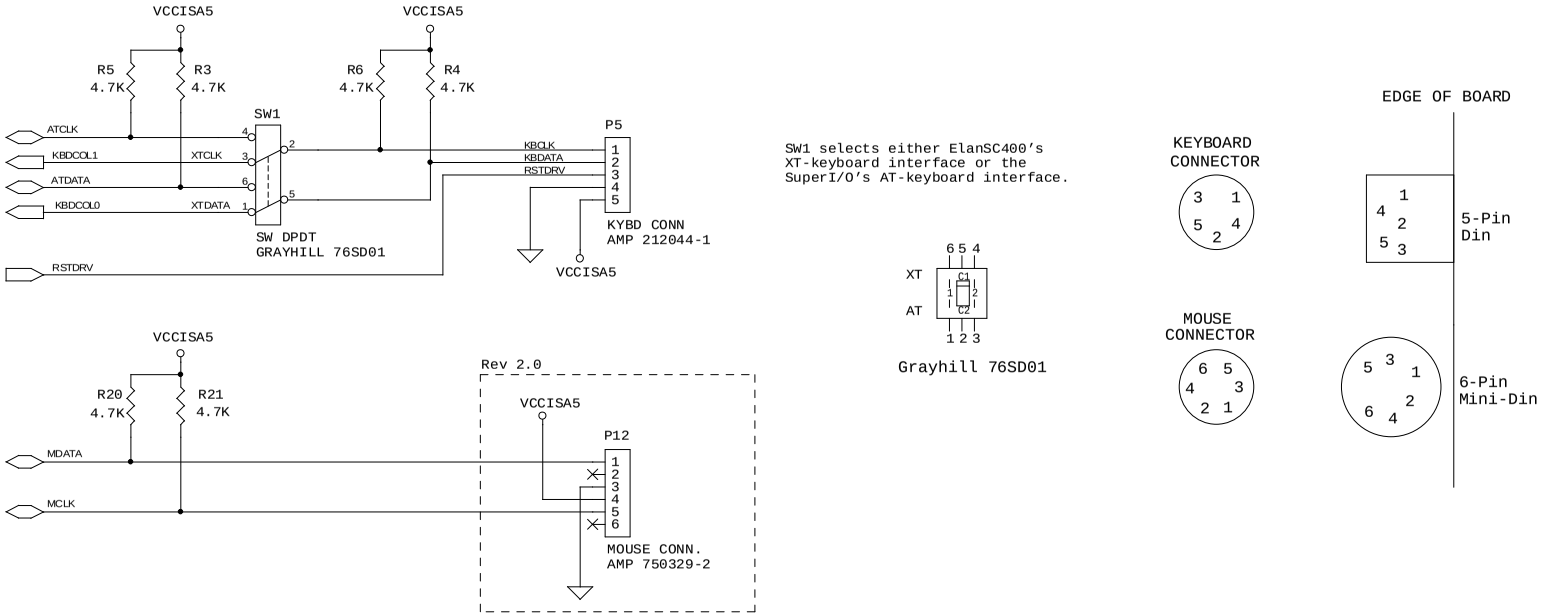

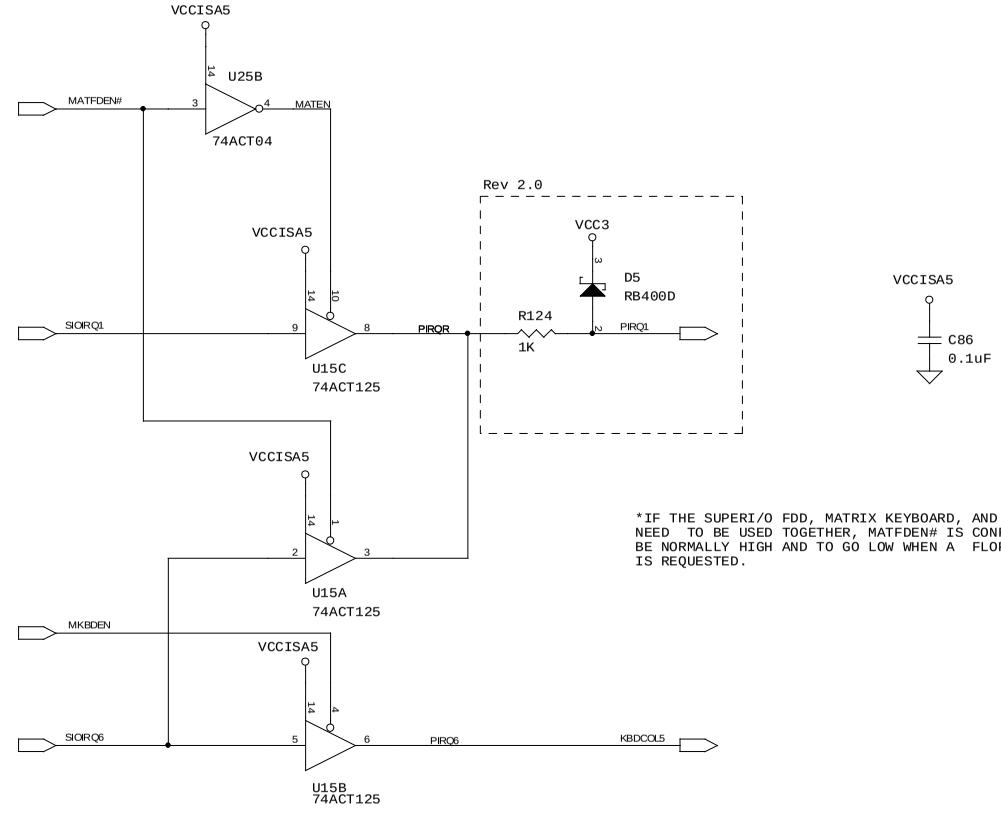

*IF THE SUPERI/O FDD, MATRIX KEYBOARD, AND AT-KEYBOARD NEED TO BE USED TOGETHER, MATFDEN# IS CONFIGURED TO BE NORMALLY HIGH AND TO GO LOW WHEN A FLOPPY ACCESS IS REQUESTED.

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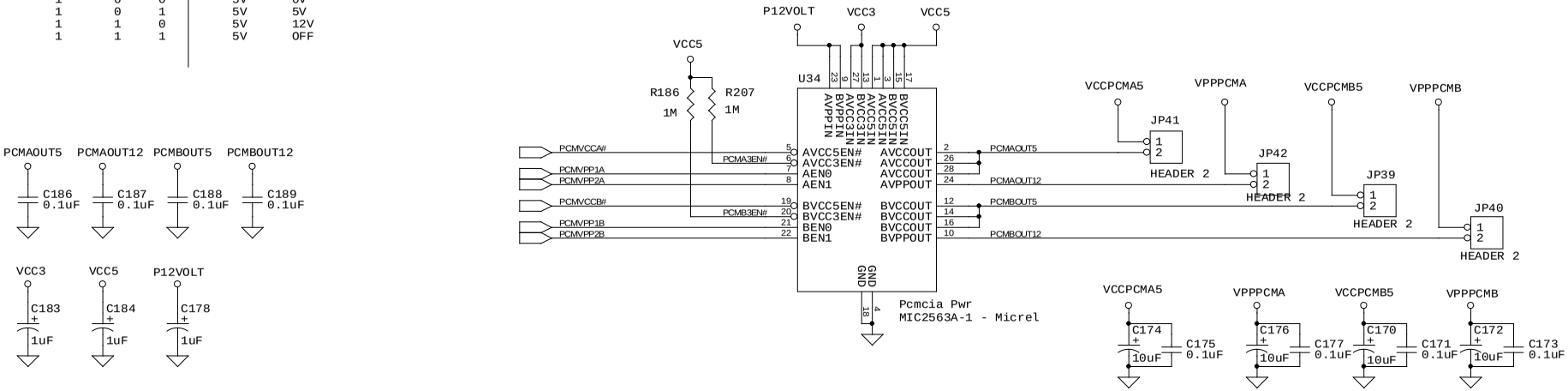
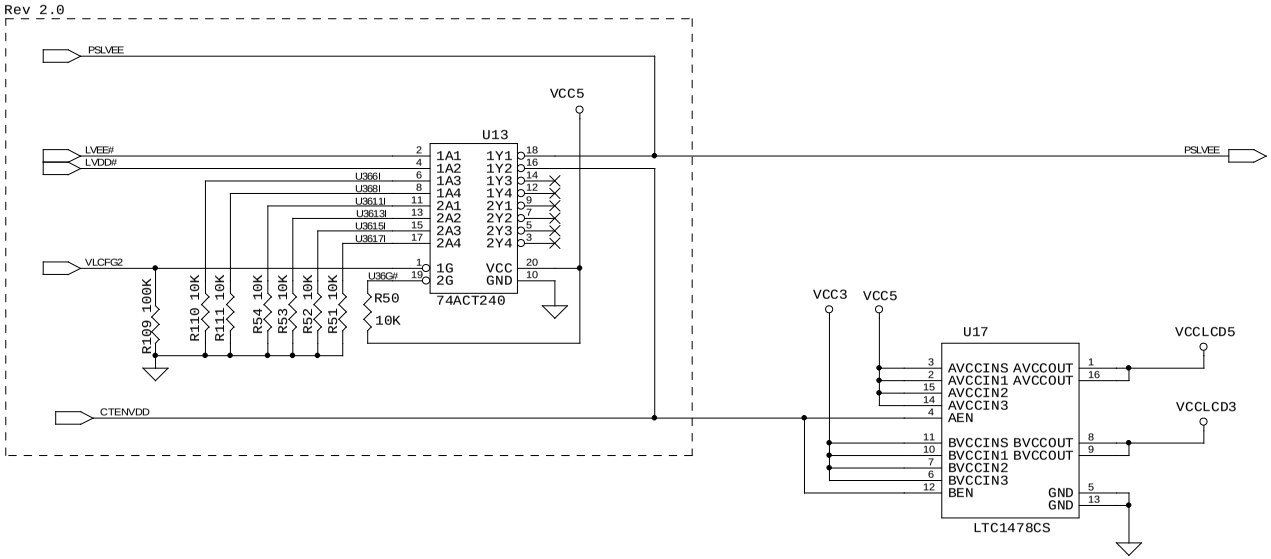
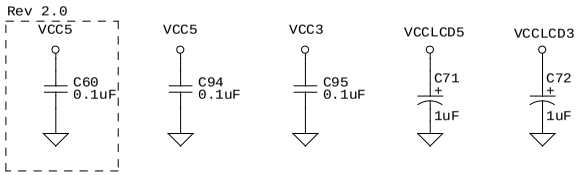
XVCC5EN#	XVCC3EN#	XEN1	XEN0	XVCCOUT	XVPPOUT
0	1	0	0	5V	0V
0	1	0	1	5V	5V
0	1	1	0	5V	12V
0	1	1	1	5V	OFF





When a VL card is installed, VLCFG2 is pulled high to tristate the outputs of the U13. CTENVDD & CTENVEE will then control VCCLCDx & VEEx.



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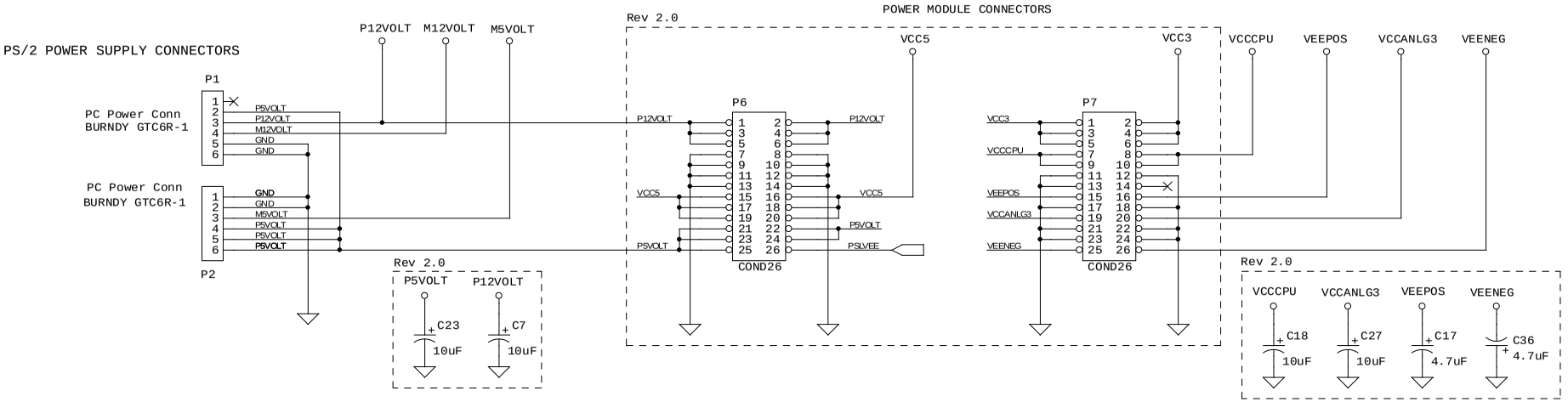

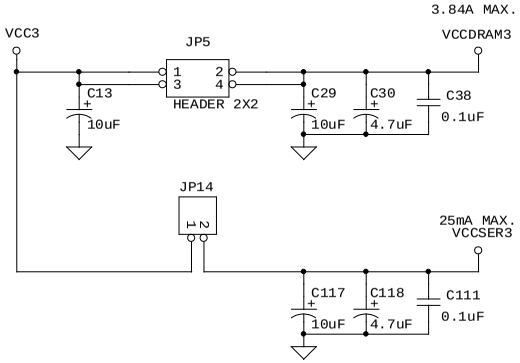

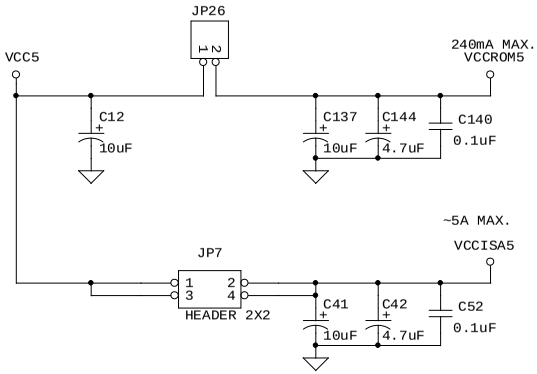

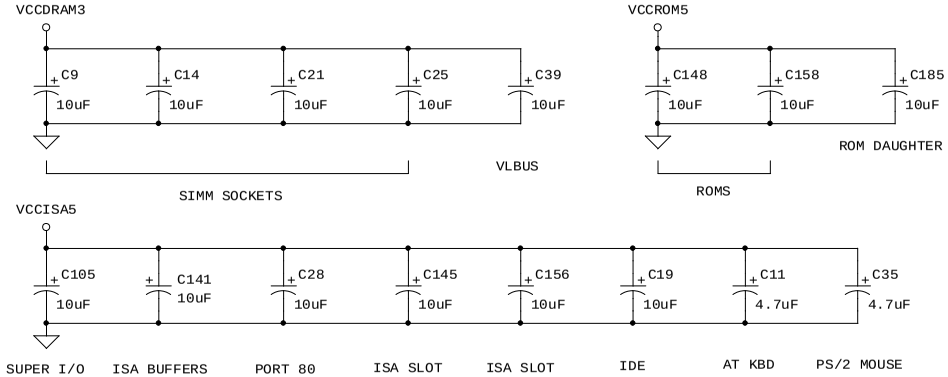

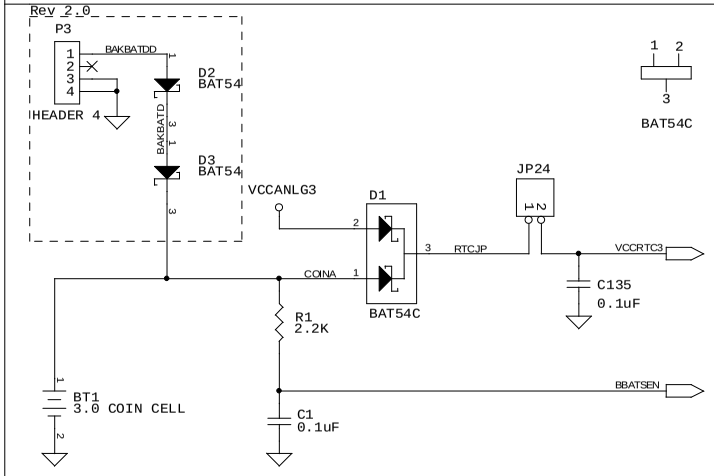

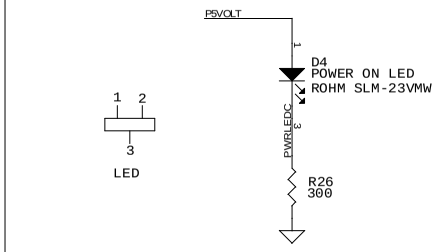

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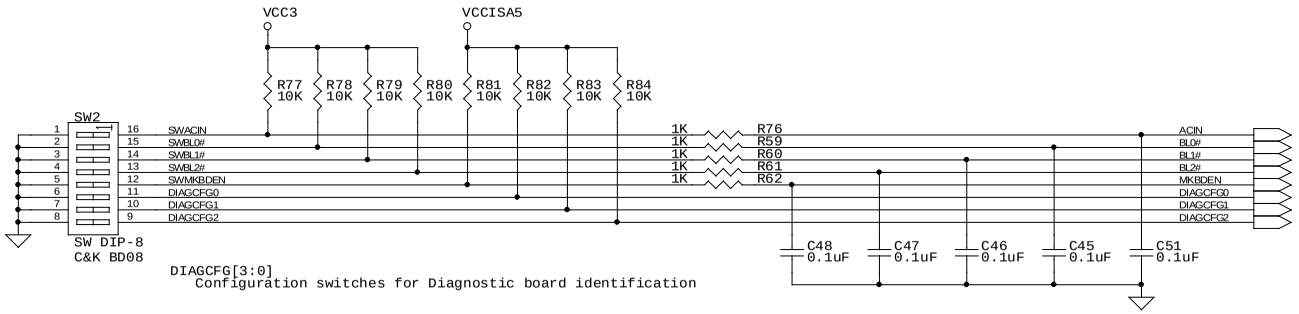
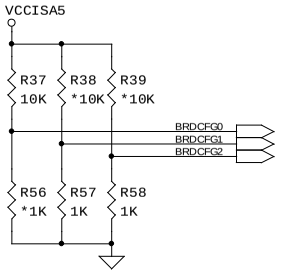
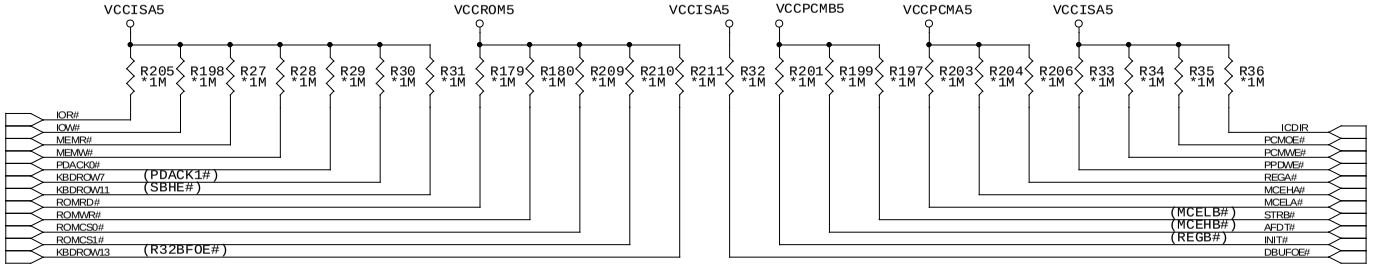


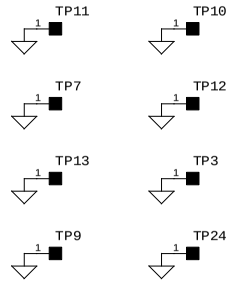
DIAGCFG[3:0]
Configuration switches for Diagnostic board identification

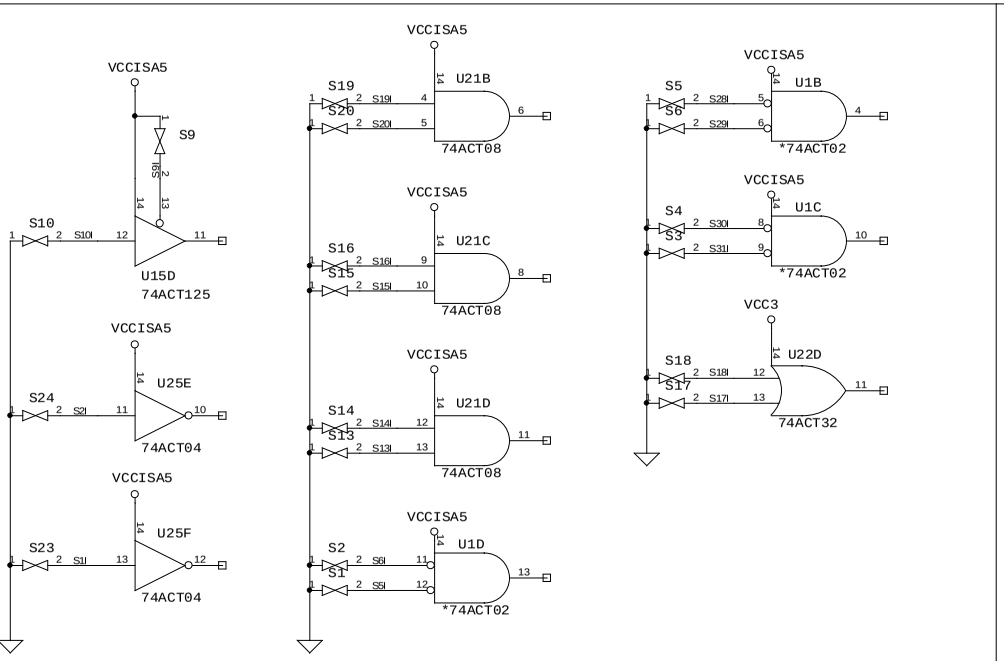


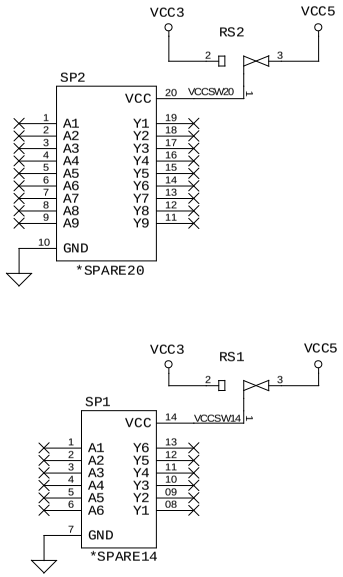
BRDCFG[2:0]:
Identifies the Revision of the board

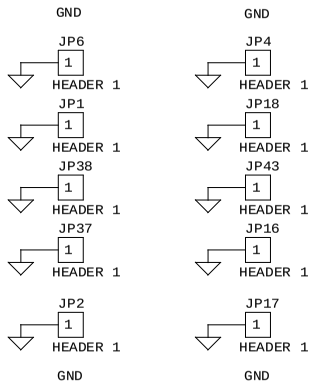


NOTE:
These pullups are used for verification testing only. They will be used when system is in SUSPEND mode.









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